Q.P. Code:**16EC5508** **R16**

Reg. No. | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
M.Tech I Year I Semester Regular & Supplementary Examinations February 2018
HARDWARE SOFTWARE CO-DESIGN
(VLSI)

Time: 3 hour Max. Marks:60

(Answer all Five Units **5 X 12 =60** Marks)

UNIT-I

1	a.	Define concurrency and identify types of concurrency	6M
	b.	Write about reactive system Co-synthesis methodology	6M
		OR	
2	a.	Demonstrate how HCFSM model support hierarchy and concurrency	8M
	b.	Illustrate CISC, RISC and VLIW architectures	4M

UNIT-II

3	a.	Present different design flow integrations for emulation	6M
	b.	Write short notes on system communication infrastructure	6M
		OR	
4	a.	What is system specialization and elucidate system specialization techniques in detail	8M
	b.	Discuss Steps involved in High level Synthesis	4M

UNIT-III

5	a.	Write a short notes on compiler validation and discuss various validation strategies	8M
	b.	Illustrate design tool requirement for embedded processors	6M
		OR	
6	a.	Discuss retarget able compiler concept	6M
	b.	Summarize practical considerations in choosing compiler development environment for embedded systems	6M

UNIT-IV

7	a.	Classify coordinating concurrent computation mechanisms	6M
	b.	Define Design, Co-design & Co-design computation models	6M
		OR	
8	a.	Discuss in which way Synchronous and asynchronous models of concurrent computations differ	6M
	b.	Summarize various kinds of formal verification used at different stages of the design process.	6M

UNIT-V

9	a.	Write about Multi language validation approaches	7M
	b.	List characteristics of Lycos system	5M
		OR	
10	a.	Draw and describe each step in COSYMA design flow	8M
	b.	Contrast homogenous to heterogeneous system level specification schemes	4M

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